AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method ~~of~~ for recording test information to identify ~~a location~~ locations of errors in integrated circuits (ICs), comprising:

scanning ~~a plurality of~~ ICs with an input signal, each IC having ~~a plurality of~~ data locations;

comparing ~~an output response at each data location~~ outputs at locations with ~~an~~ expected values ~~value~~ for the data locations ~~location~~; and

storing addresses in a buffer for ~~each data location~~ data locations at which an output ~~the response at the data location~~ does not equal ~~the~~ an expected value;

wherein, after a pre-determined number of addresses are stored in the buffer, addresses for data locations at which an output does not equal an expected value are not stored in the buffer ~~corresponding to the data location~~.

2. (Currently Amended) The method of claim 1, further comprising sending a data string containing the addresses stored in the buffer to a storage device ~~containing the addresses~~.

3. (Currently Amended) ~~The method of claim 2,~~ A method for recording test information to identify locations of errors in integrated circuits (ICs), comprising:

scanning ICs with an input signal, each IC having data locations;

comparing output at locations with expected values for the data locations; and

storing addresses in a buffer for data locations at which an output does not equal an expected value not stored in the buffer;

sending a data string containing the addresses stored in the buffer to a storage device;

wherein sending the data string comprises ~~includes~~:

(i) sending a header containing an x-address, a y-address, and a scan-address for each of the data locations;

(ii) sending device addresses; and

(iii) sending a trailer.

4. (Currently Amended) The method of claim 3, wherein ~~a series of~~ the device addresses comprises ~~includes sending~~ an extension.

5. (Currently Amended) The method of claim 2, wherein sending the data string comprises ~~includes~~:

sending a header containing an x-address, a device address, and a scan address for each of the data locations;

sending ~~a series of~~ y-addresses; and

sending a counter having a count of y-addresses.

6. (Currently Amended) The method of claim [~~1~~]2, wherein sending the data string ~~addresses~~ comprises ~~includes~~ sending a memory address and a location of the IC.

7. (Currently Amended) The method of claim 1, further comprising placing the ICs on a burn-in board and scanning the ICs with the input signal in order to determine defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value;

wherein placing the ICs on the burn-in board comprises arranging the ICs in columns and rows, the columns being connected in parallel with other columns and being configured to receive the input signal through the data locations..

8. (Currently Amended) The method of claim 1, further comprising

leaving the ICs on a wafer and scanning the ICs with the input signal in order to determine defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value..

9. (Currently Amended) The method of claim 1, ~~further comprising using memory cells as~~ wherein the data locations comprise memory cells.

10. (Cancelled).

11. (Currently Amended) The method of claim 1, further comprising filtering out defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value;

wherein the filtering comprises:

locating the defective ICs on a burn-in board or a wafer;

repairing the defective ICs;

removing non-defective ICs from the burn-on board or the wafer, the non-defective ICs corresponding to data locations at which the output equals the expected value; and

storing the non-defective ICs into packages.

12. (Currently Amended) A system ~~of~~ for recording test information to identify a location of an error for integrated circuits (ICs), comprising:

at least one comparator ~~comparing~~ to compare ~~an output response~~ outputs at ~~each of a plurality of data~~ locations ~~in a plurality of ICs~~ with ~~an~~ expected values for the data locations ~~value corresponding to the data locations~~; and

a processor ~~scanning~~ to scan the at least one comparator at ~~each~~ data locations ~~location~~ and ~~the processor sending~~ to store addresses to a buffer when ~~the response at each data location~~ an output for data locations does not equal ~~the~~ an expected value;

wherein, after a pre-determined number of addresses are stored in the buffer, addresses for data locations at which an output does not equal an expected value are not stored in the buffer.

13. (Currently Amended) The system of claim 12, further comprising a data storage device that receives ~~the~~ addresses from the processor in a data string.

14. (Currently Amended) ~~The system of claim 13,~~ A system for recording test information to identify locations of errors for integrated circuits (ICs), comprising:

at least one comparator comparing outputs at locations with expected values for the data locations; ~~and~~

a processor to scan at least one comparator at data locations and to store addresses to a buffer when an output for data locations does not equal an expected value; and

a data storage device that receives addresses from the processor in a data string;

wherein the data string comprises ~~includes~~:

(i) a header containing an x-address, a y-address, and a scan-address for each of the data locations;

(ii) device addresses; and

(iii) a trailer.

15. (Original) The system of claim 14 wherein each device address includes an extension.

16. (Currently Amended) The system of claim 13, wherein the data string comprises ~~includes~~:

a header containing an x-address, a device address, and a scan address for each of the data locations;

y-addresses; and

a counter having a count of y-addresses.

17. (Currently Amended) The system of claim ~~12~~13, wherein the addresses comprises ~~includes~~ a memory address and a location of the IC.

18. (Currently Amended) The system of claim 12, wherein the ICs are placed on a burn-in board and scanned with the input signal in order to determine defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value;

wherein placing the ICs on the burn-in board comprises arranging the ICs in columns and rows, the columns being connected in parallel with other columns and being configured to receive the input signal through the data locations.

19. (Currently Amended) The system of claim 12, wherein the ICs are placed on a wafer and scanned with the input signal in order to determine defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value

20. (Currently Amended) The system of claim 12, wherein the data locations comprise ~~are~~ memory cells.

21. (Currently Amended) The system of claim 12, further comprising a data stack being connected to the comparator, the data stack being configured to:

determine a quantity of failures for each of the ICs on the burn-in board or the wafer;

replace an ICs with a redundant element after the quantity of failures for the IC exceeds a threshold.

22. (Currently Amended) The system of claim 12, further comprising a ~~fail~~ logic mask, the logic mask comprising a bit map and being configured to prevent the recording of irrelevant information from defective ICs, the defective ICs corresponding to data locations at which the output does not equal the expected value.